Enabling Envelope Tracking through GaN Transistors

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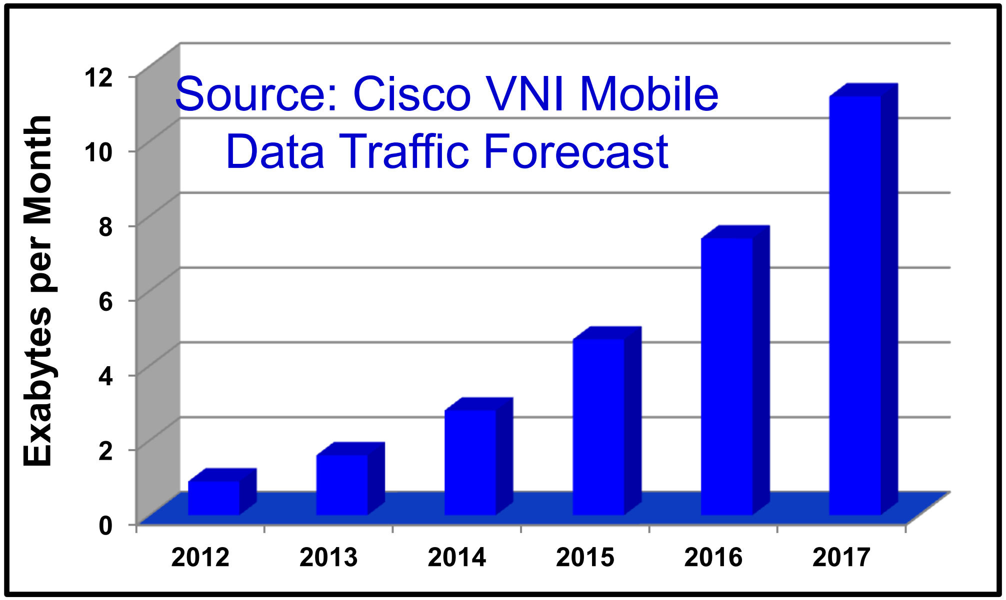
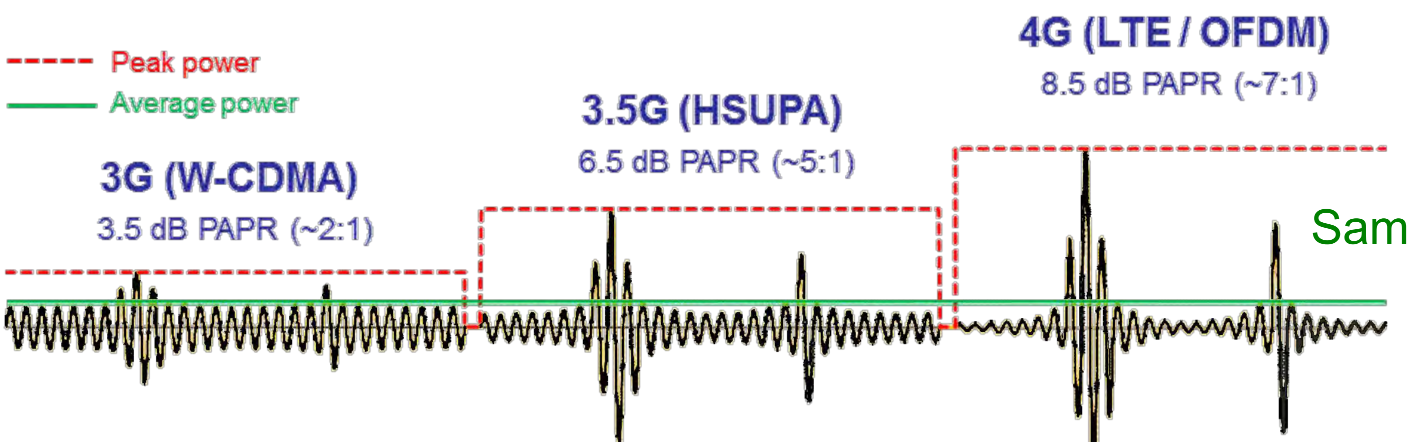
Agenda

- Overview of Envelope Tracking
- Why eGaN® FETs for Envelope Tracking
- Maximizing Device Performance
- Experimental Results
- Summary and Current Limitations
- A Look into the Future
- Q & A

Why Envelope Tracking?

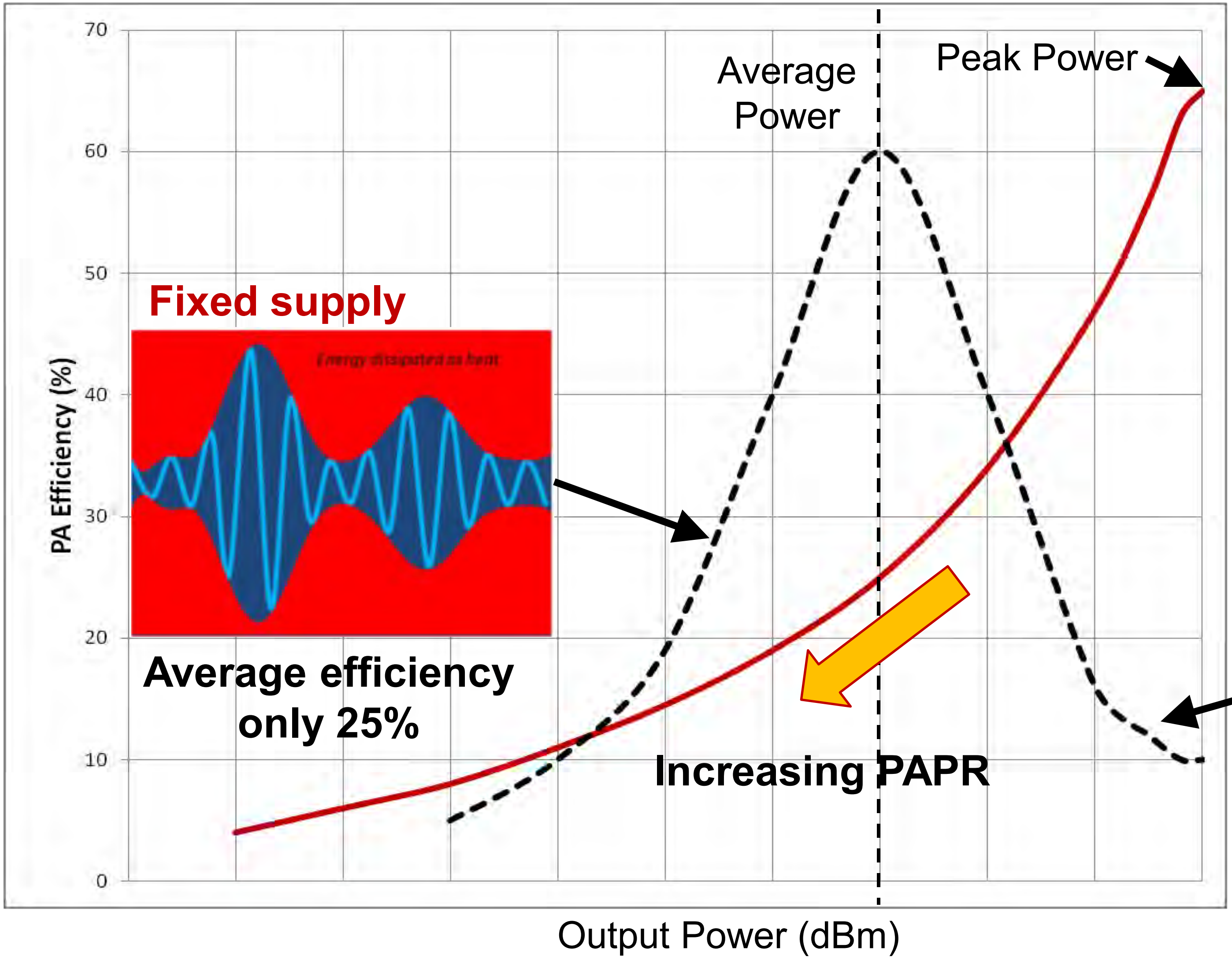


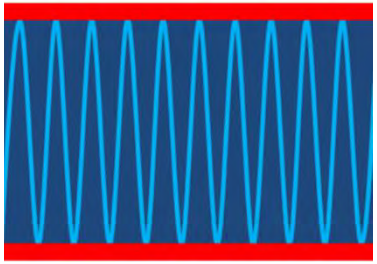
66% Compound annual growth rate (CAGR)



Reference: Nujira.com website

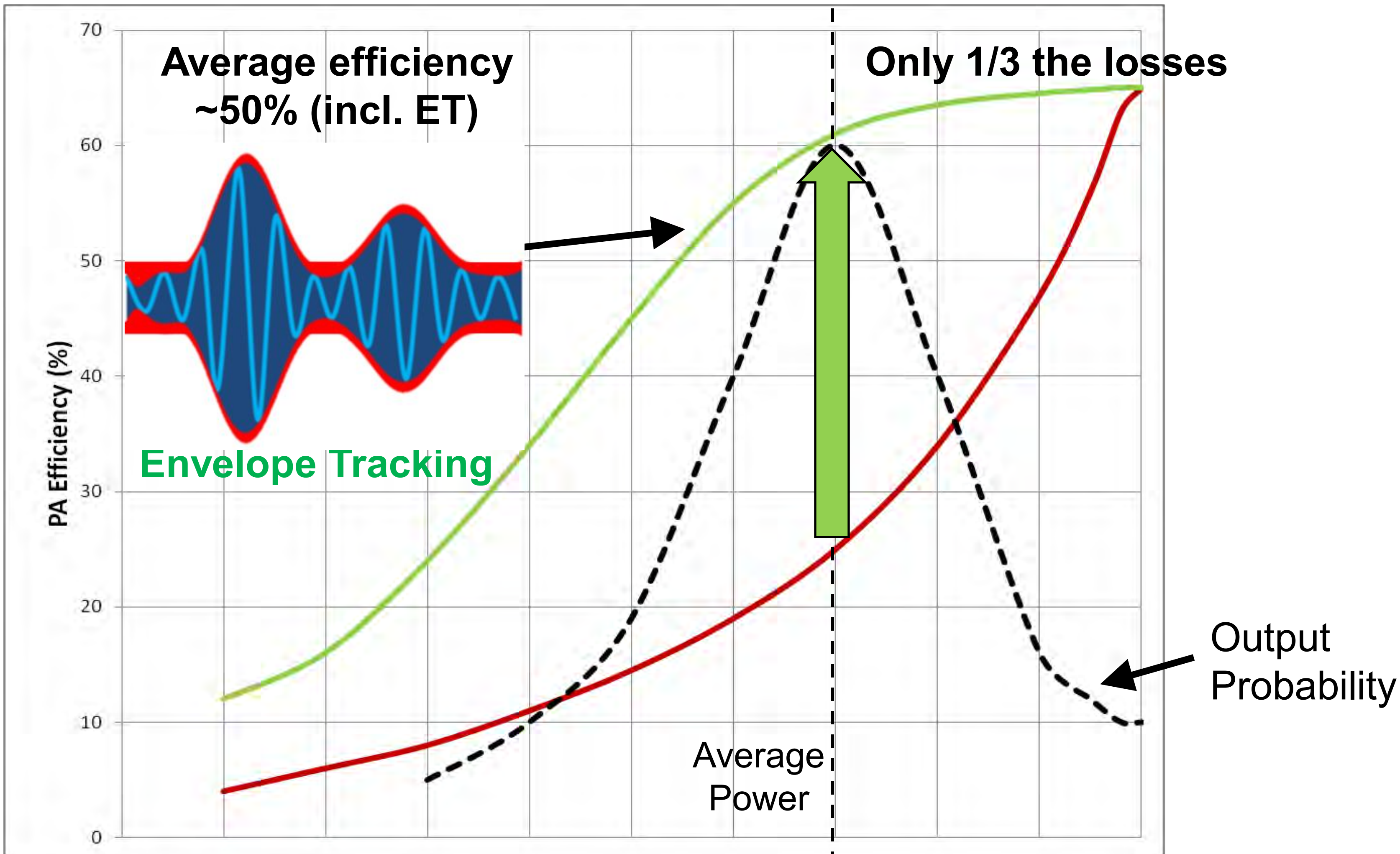
Effect of PAPR





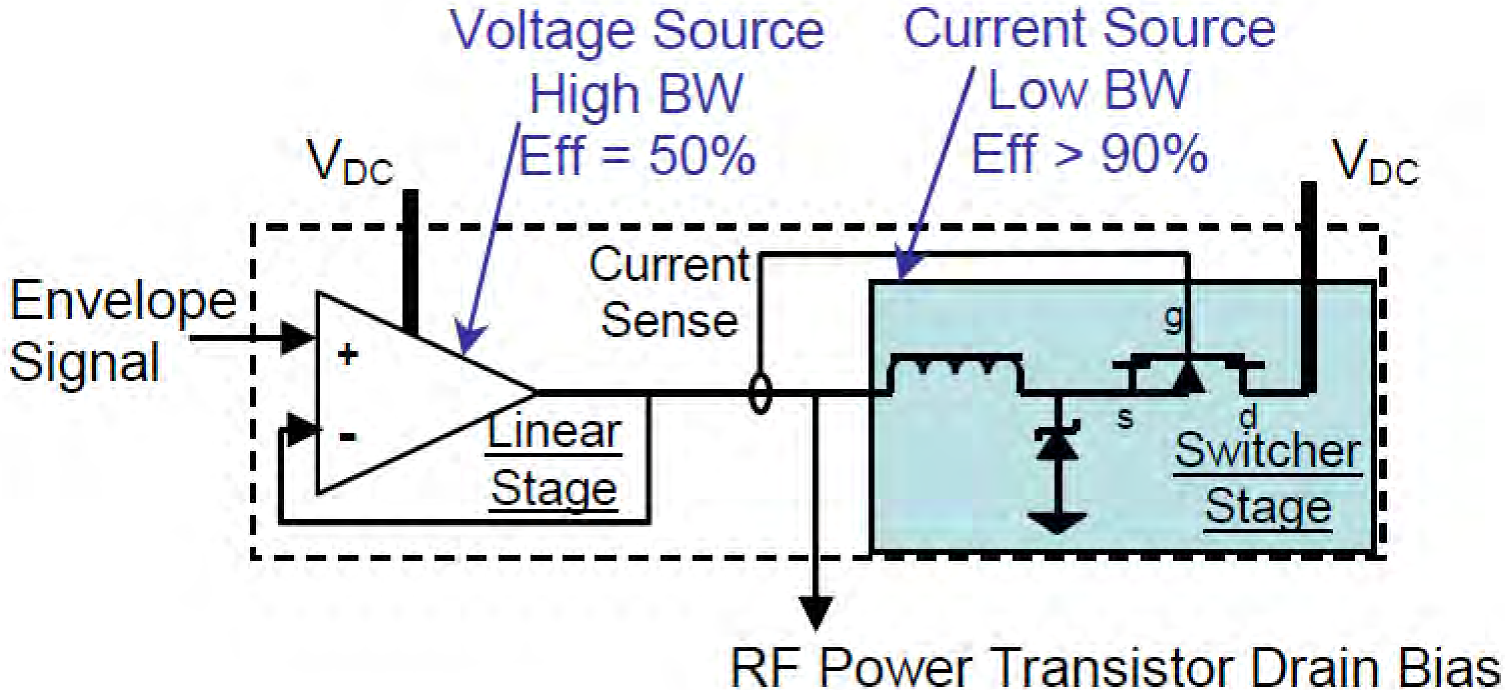
PAPR = 0dB
Peak efficiency up to 65%

Effect of Envelope Tracking



Output Power (dBm)

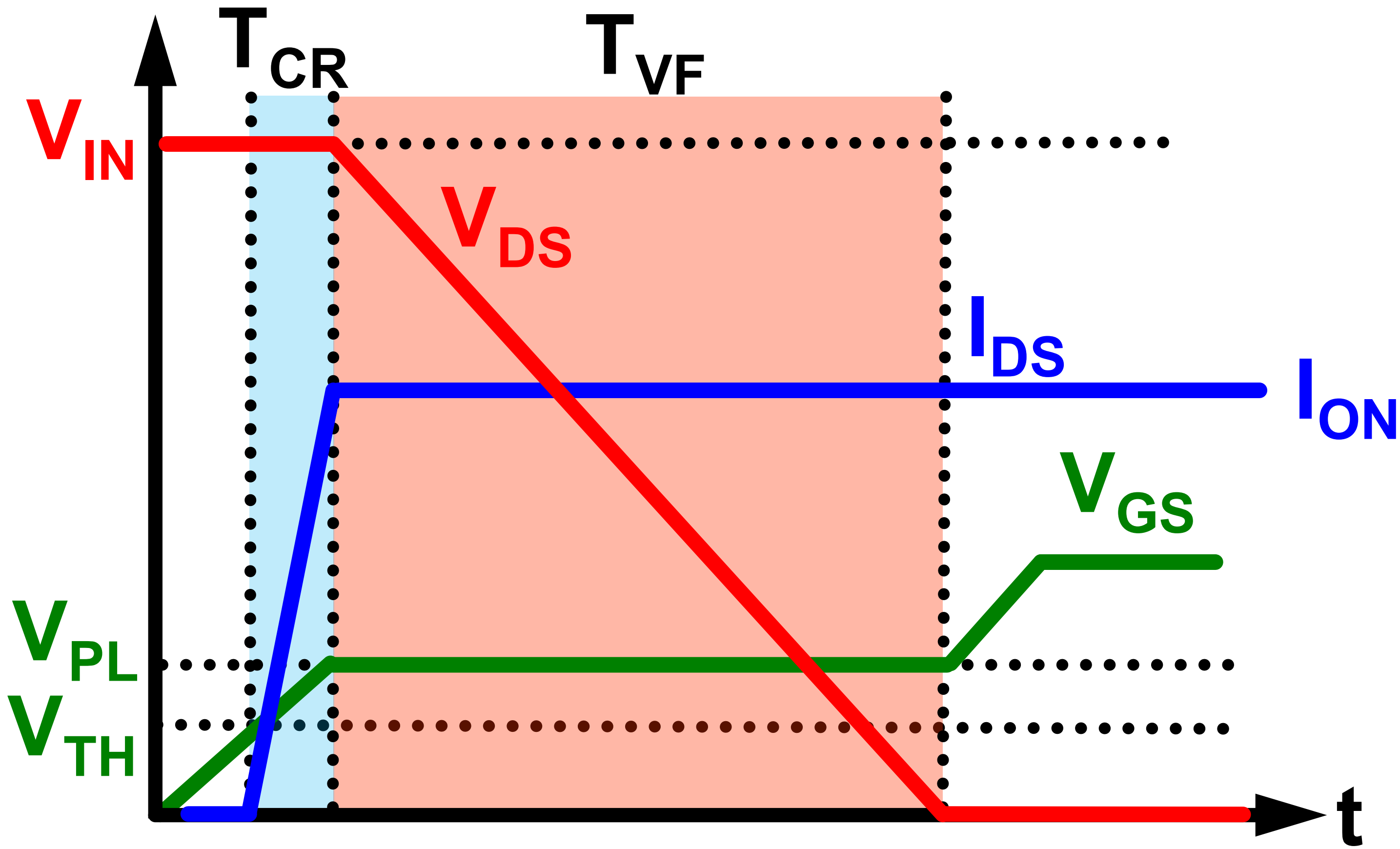
Hybrid ET Implementation



Can benefit from both improved efficiency and improved bandwidth
- Improves overall ET efficiency
- Simplifies Linear stage design / Removes it entirely?
- Increase linear stage BW – improved performance

Kimball, Don, et al. "50% PAE WCDMA basestation amplifier implemented with GaN HFETs." *Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC'05. IEEE*. IEEE, 2005.

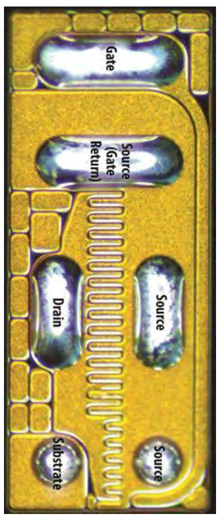
Idealized Switching



$$P_{T_{CR}} \; \alpha \; \frac{V_{IN} * I_{ON} * Q_{GS2}}{2 * I_G}$$

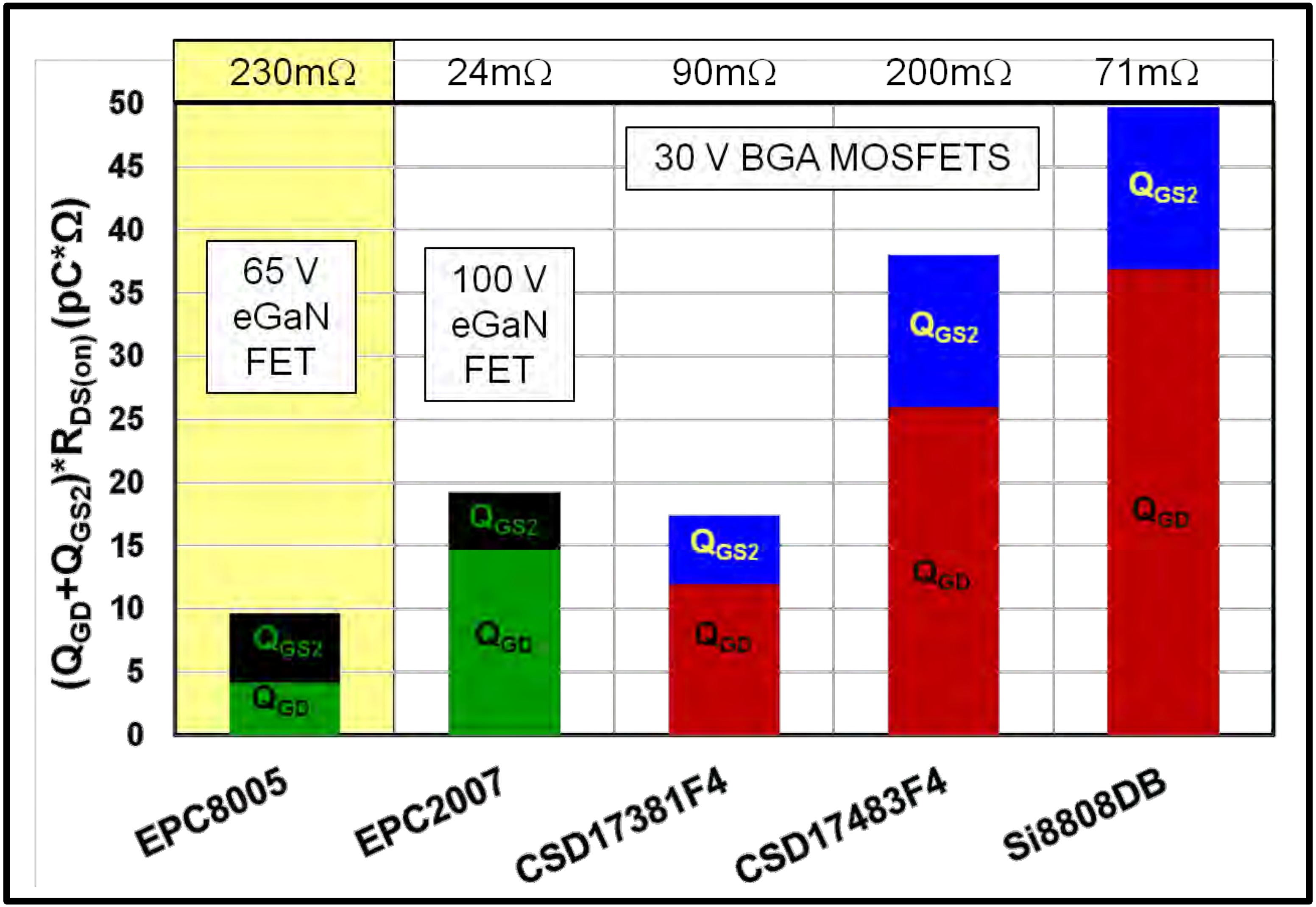
$$P_{T_{VF}} \; \alpha \; \frac{V_{IN} * I_{ON} * Q_{GD}}{2 * I_G}$$

High Frequency eGaN FETs

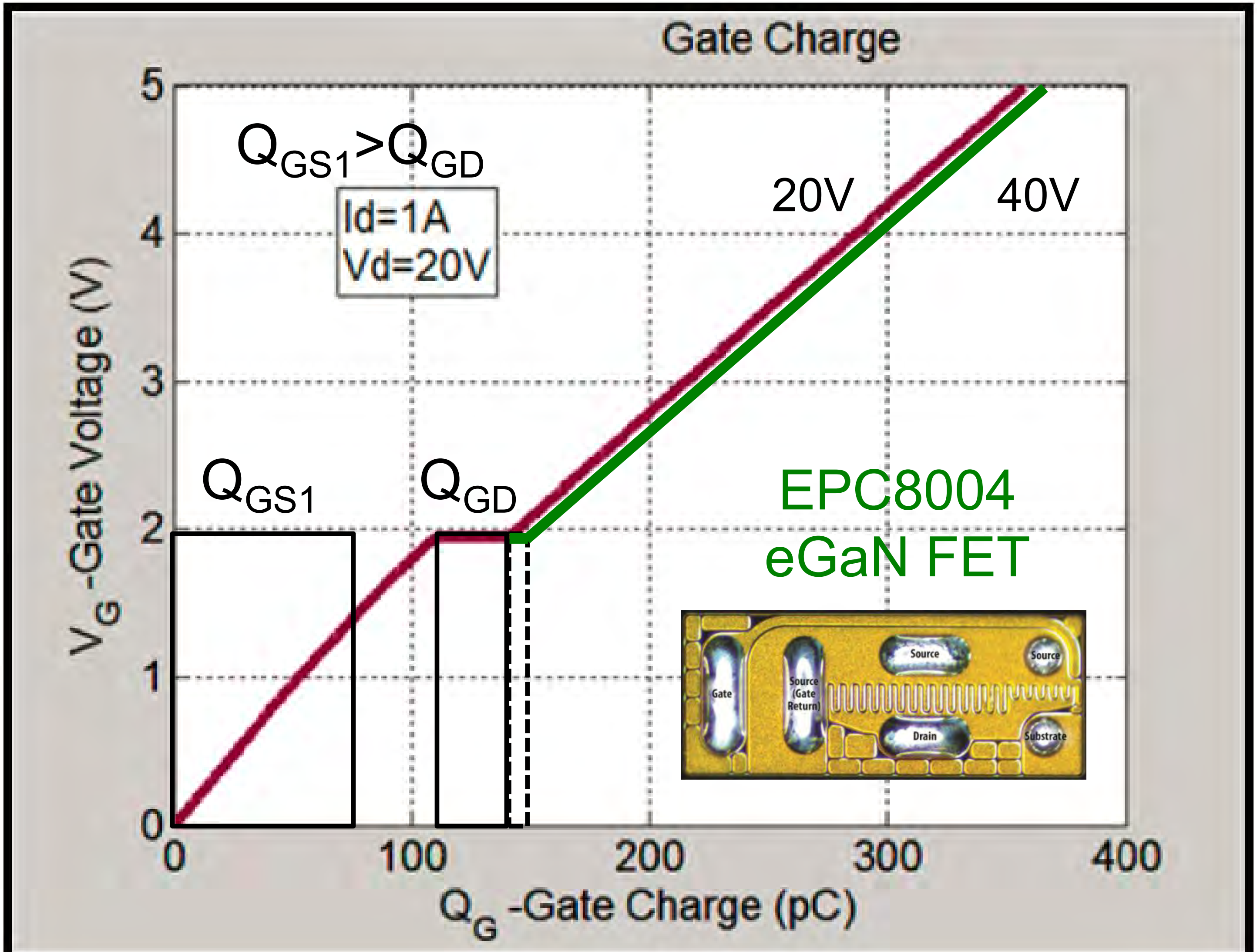


EPC Part No.	BV (V)	Max. $R_{DS(ON)}$ (mΩ) (V_{GS} = 5V, I_D = 0.5 A)	Min. Peak Id (A) (Pulsed, 25 °C, T_{pulse} = 300 µs)	Typical Charge (pC)					Typical Capacitance (pF) (V_{DS} = 20 V; V_{GS} = 0 V)		
				Q_G	Q_{GD}	Q_{GS}	Q_{OSS}	Q_{RR}	C_{ISS}	C_{OSS}	C_{RSS}
EPC8004	40	125	7.5	358	31	110	493	0	45	17	0.4
EPC8007	40	160	6	302	25	97	406	0	39	14	0.3
EPC8008	40	325	2.9	177	12	67	211	0	25	8	0.2
EPC8009	65	138	7.5	380	36	116	769	0	47	17	0.4
EPC8005	65	275	3.8	218	18	77	414	0	29	9.7	0.2
EPC8002	65	530	2	141	9.4	59	244	0	21	5.9	0.1
EPC8003	100	300	5	315	34	110	1100	0	38	18	0.2
EPC8010	100	160	7.5	354	32	109	1509	0	47	18	0.2

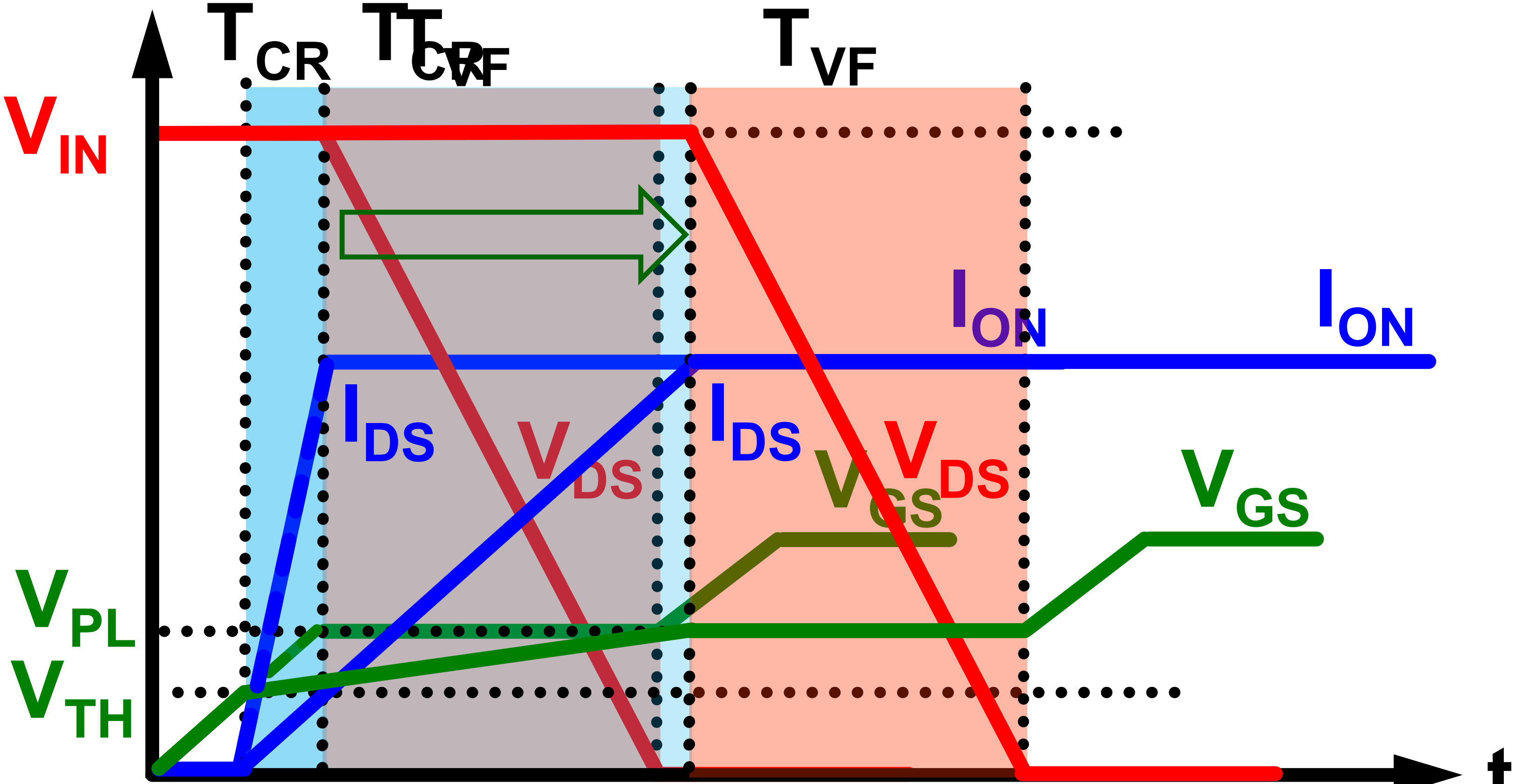
Hard Switching FOM



dv/dt Immunity



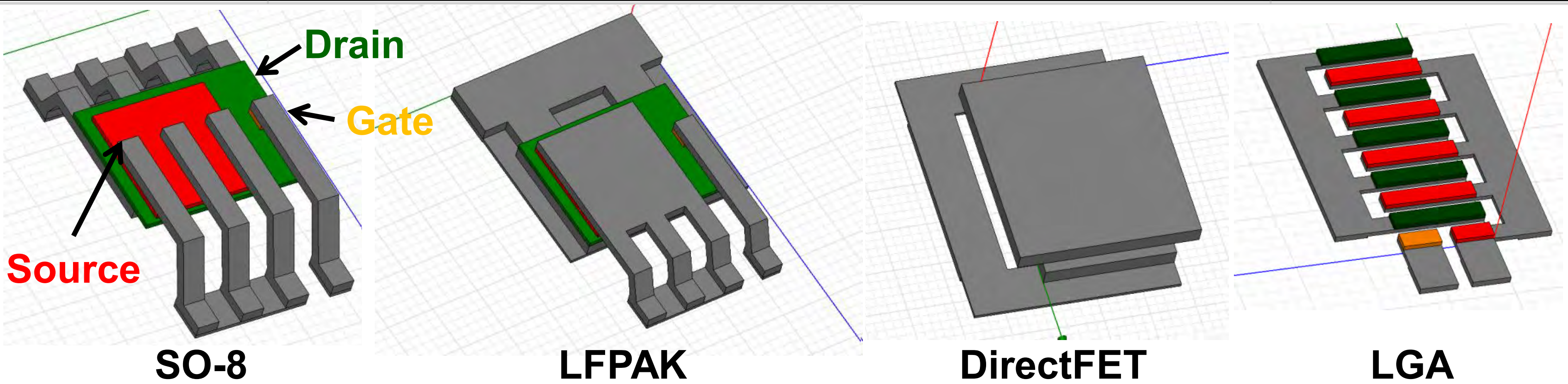
Common Source Inductance

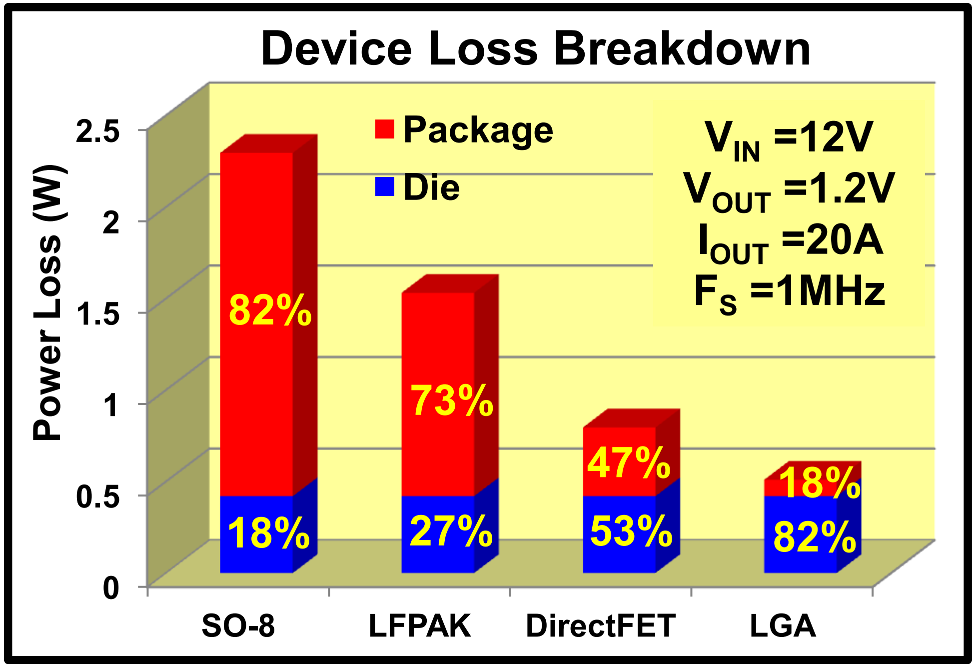


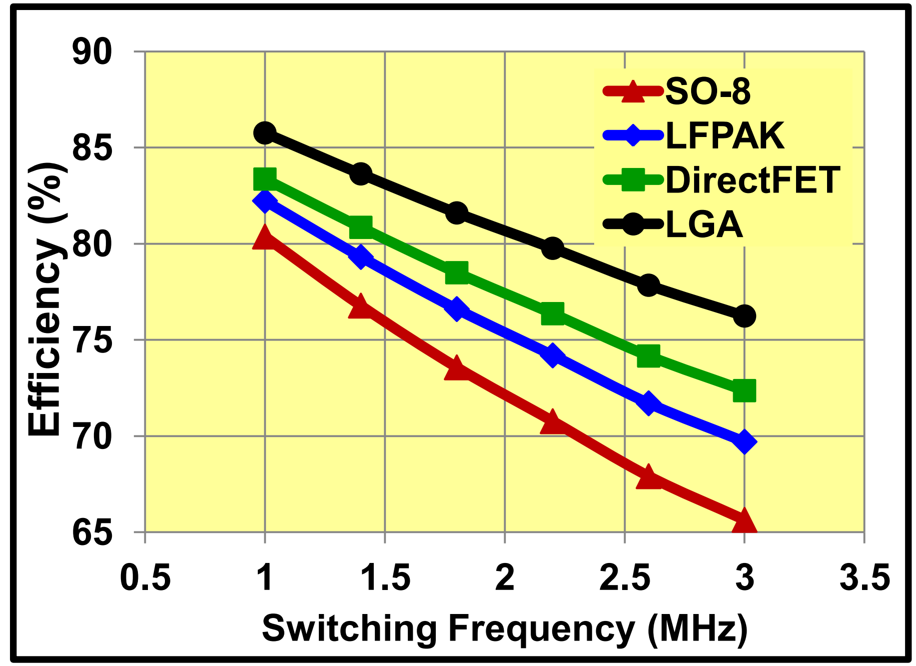
$$P_{T_{CR}} \alpha \frac{V_{IN} * I_{ON} * Q_{GS2}}{2 * I_G}$$

$$P_{T_{VF}} \alpha \frac{V_{IN} * I_{ON} * Q_{GD}}{2 * I_G}$$

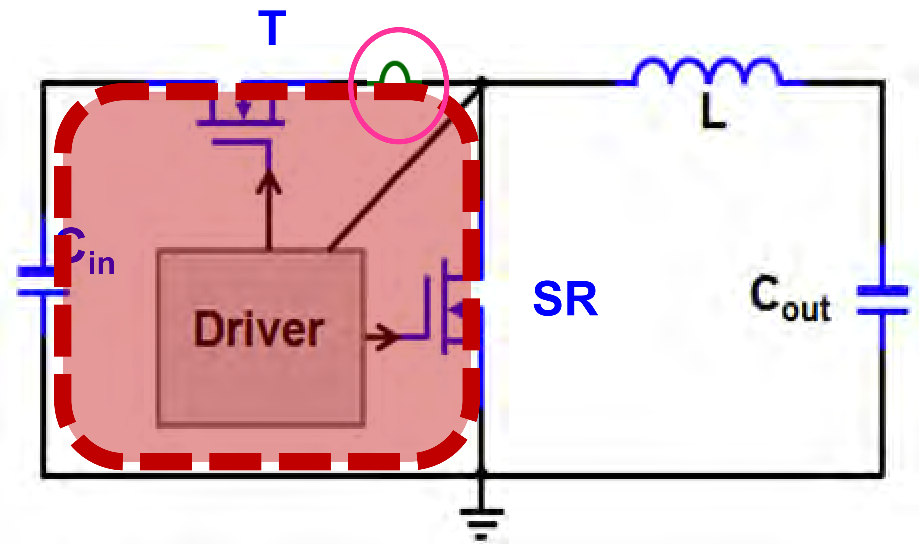
Packaging Evolution

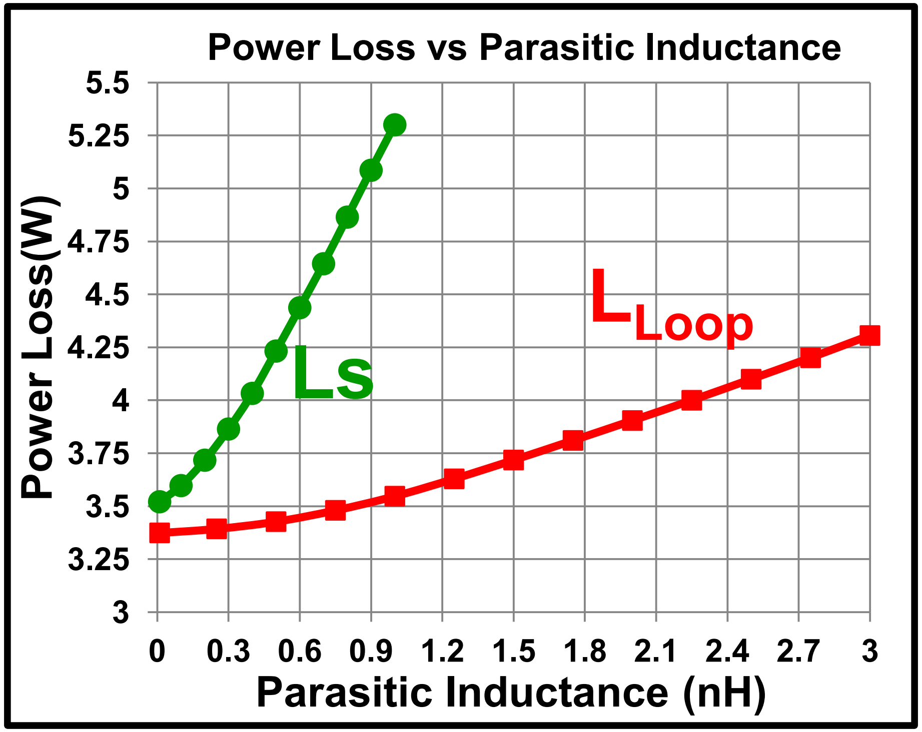






Converter Parasitics





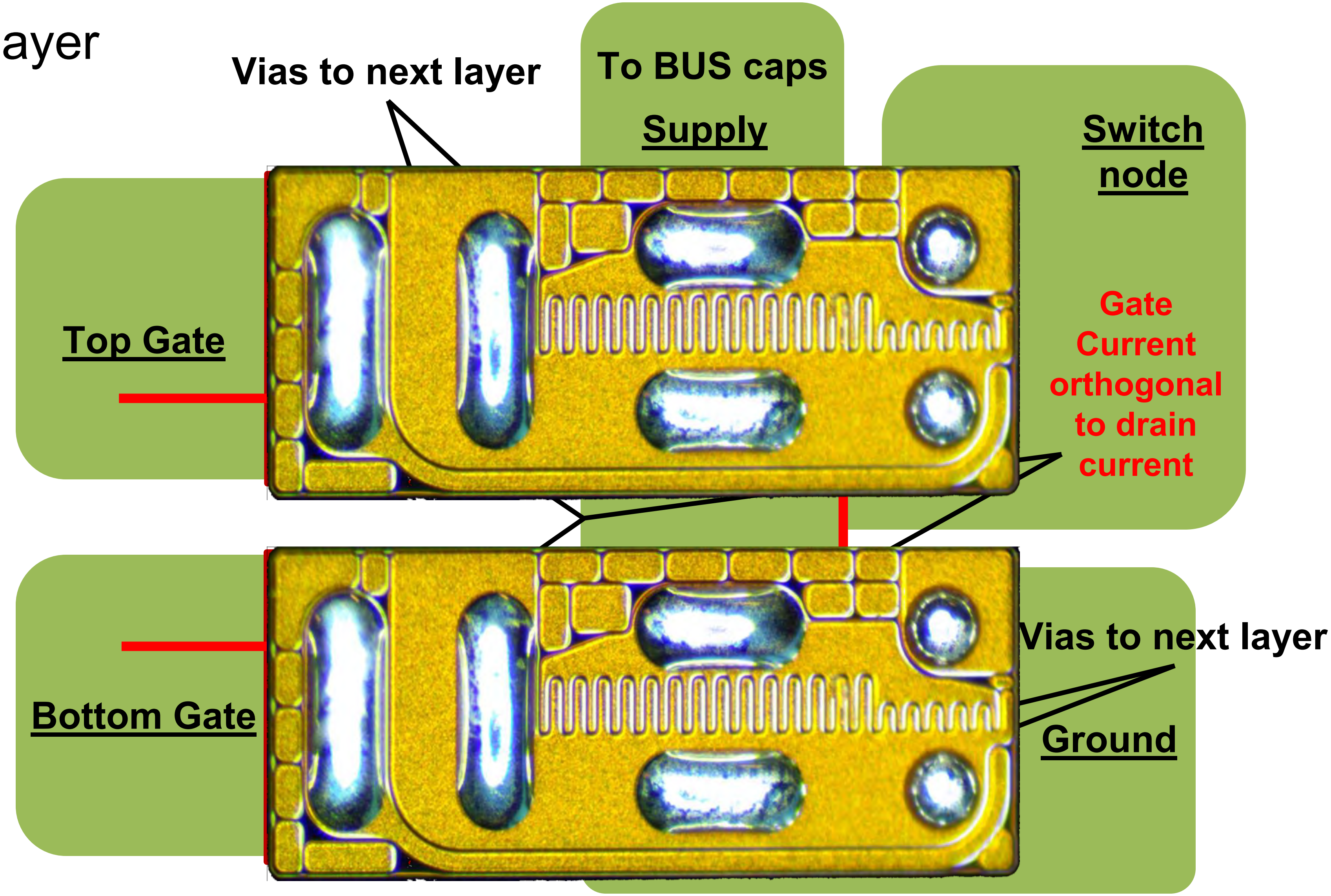
L_S: Common Source Inductance

L_{Loop}: High Frequency Power Loop Inductance

V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, I_{OUT}= 20 A

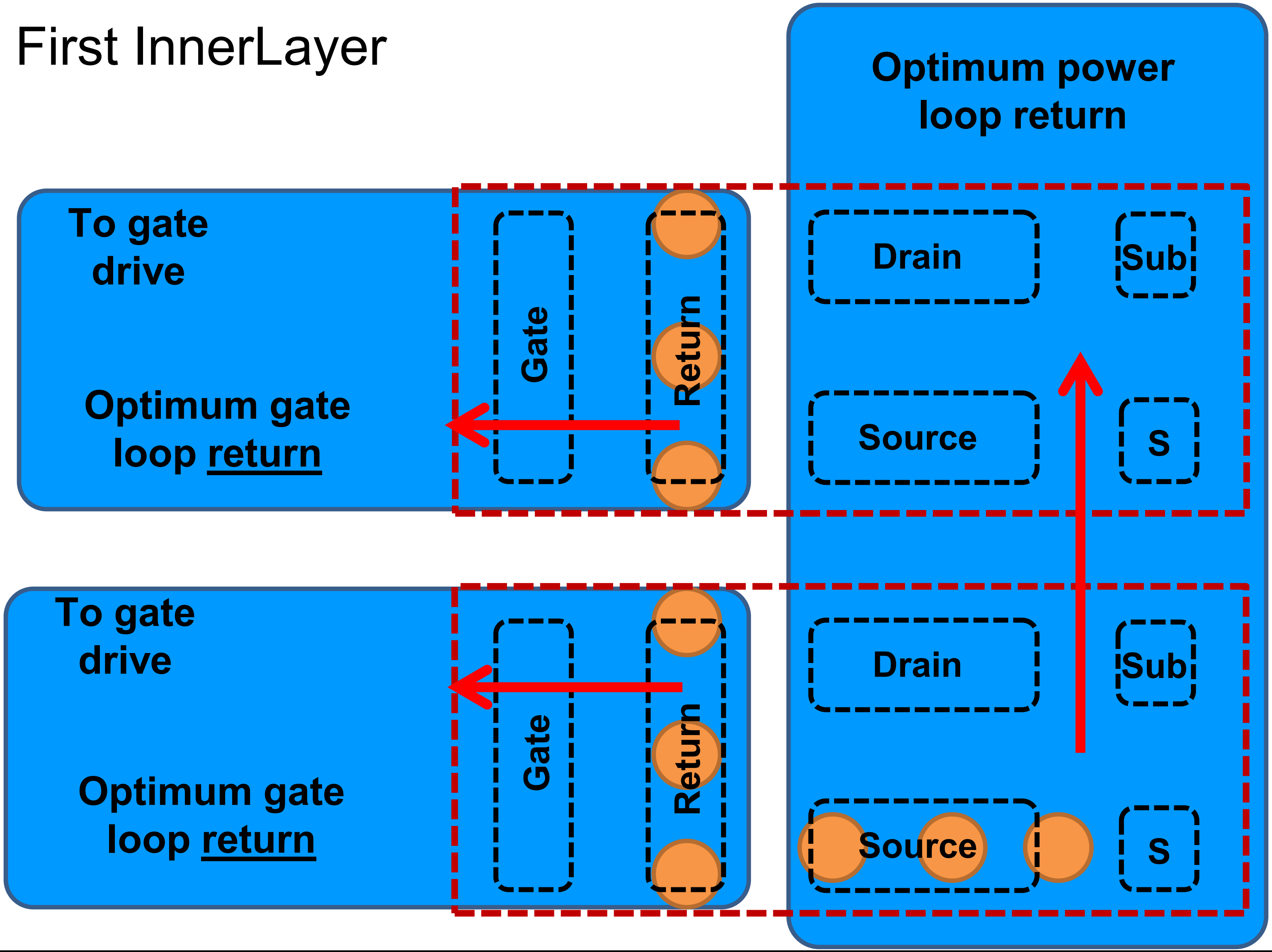
Low Parasitic Layout

Top Layer

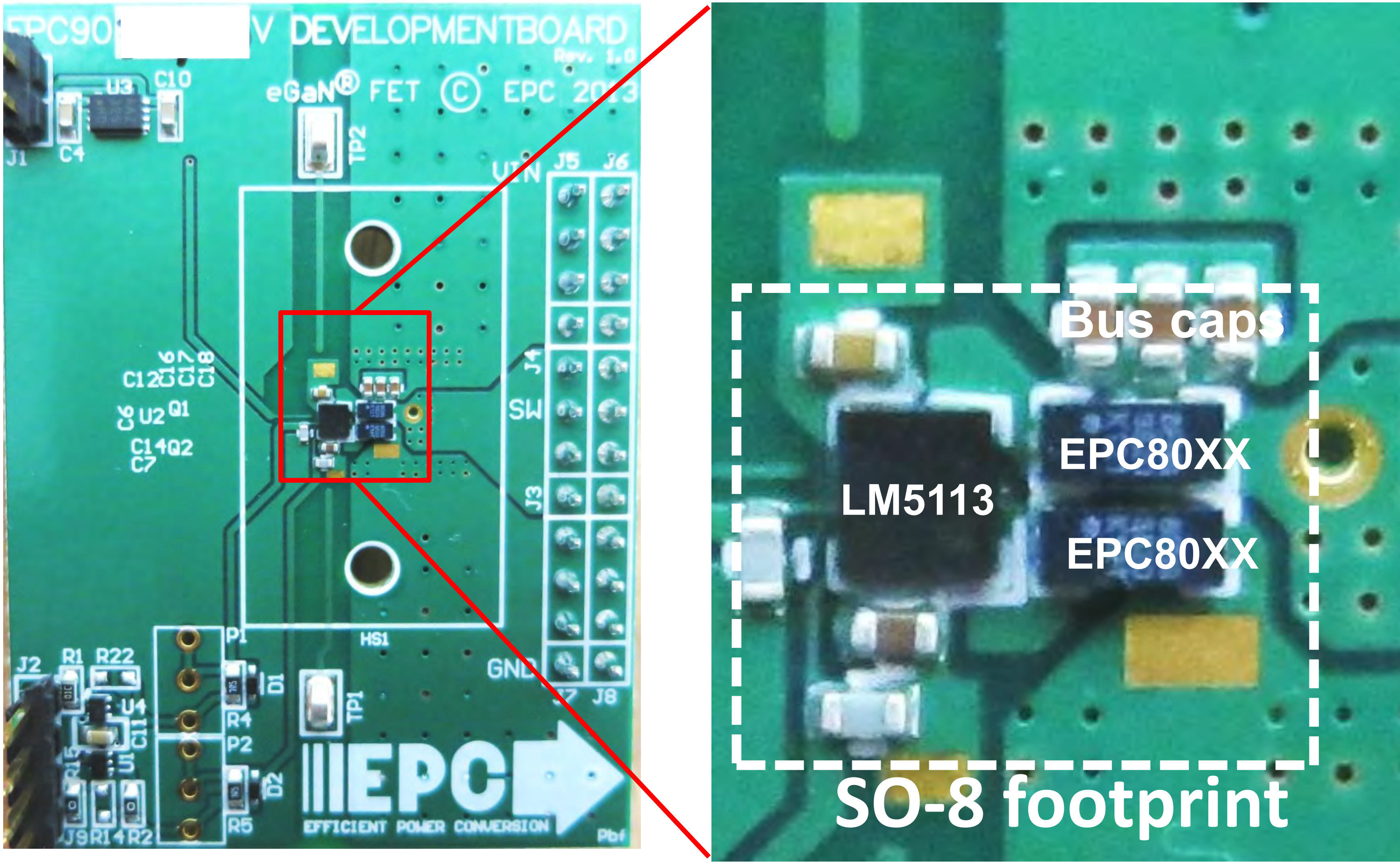


Low Parasitic Layout

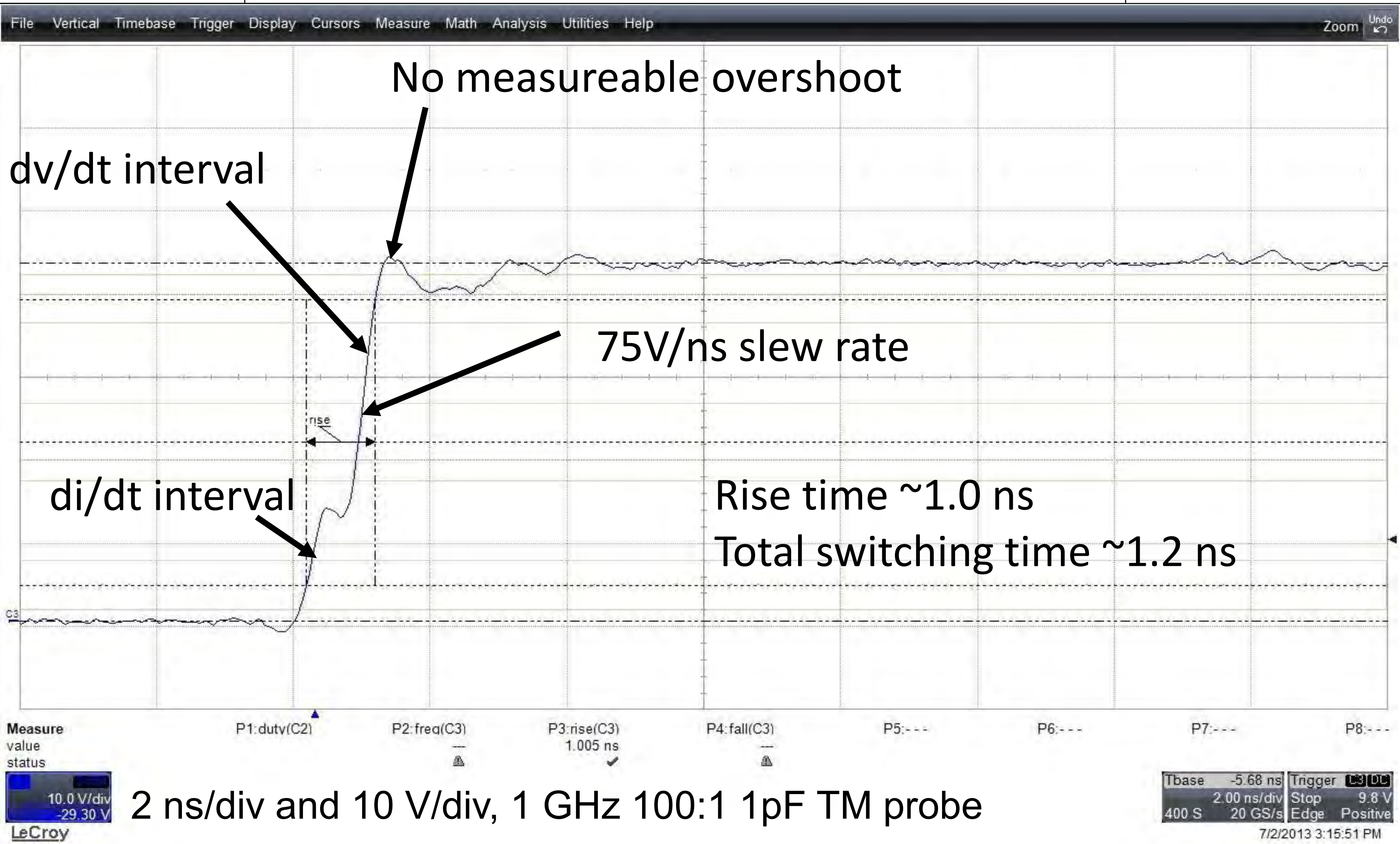
First InnerLayer



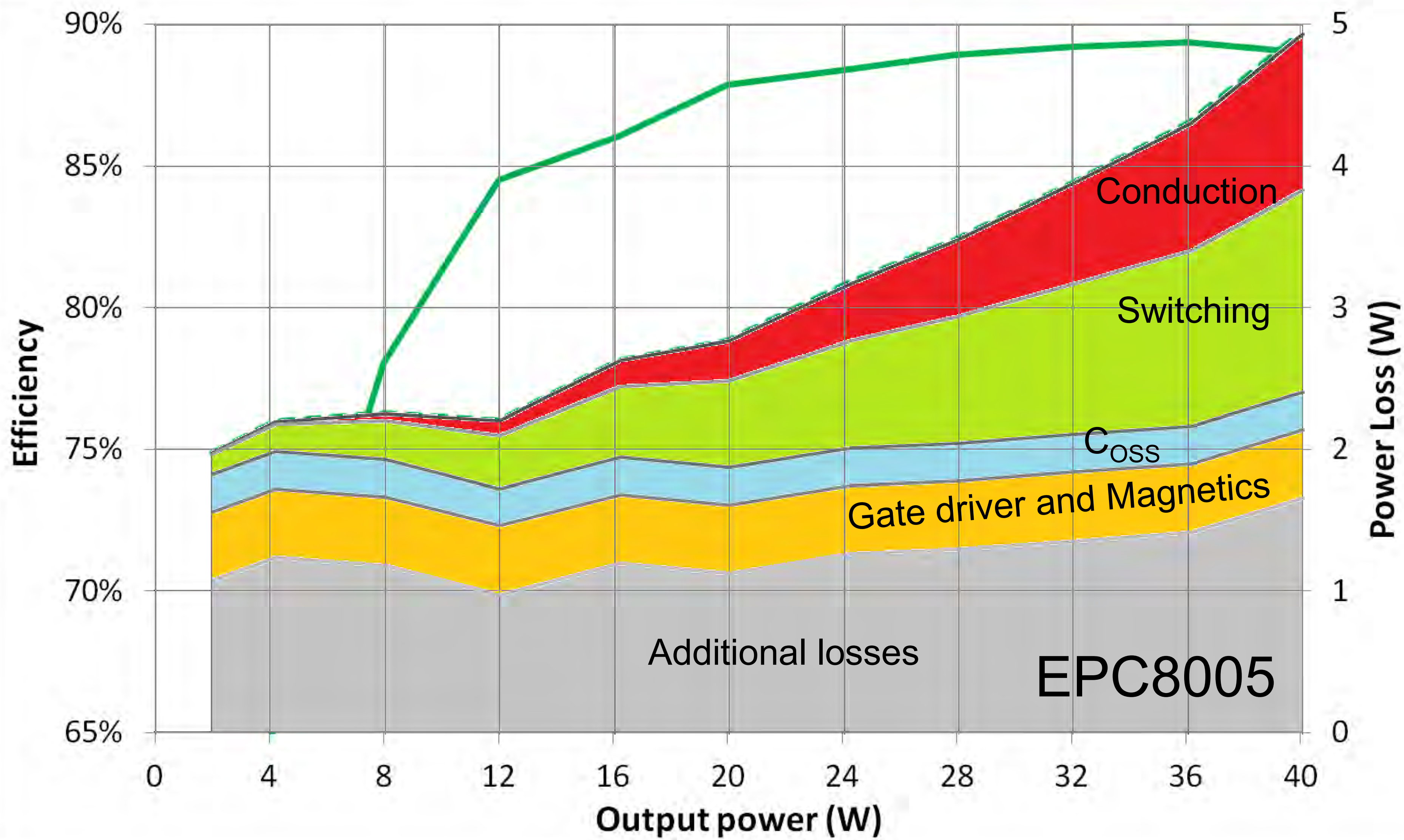
ET Prototype Board



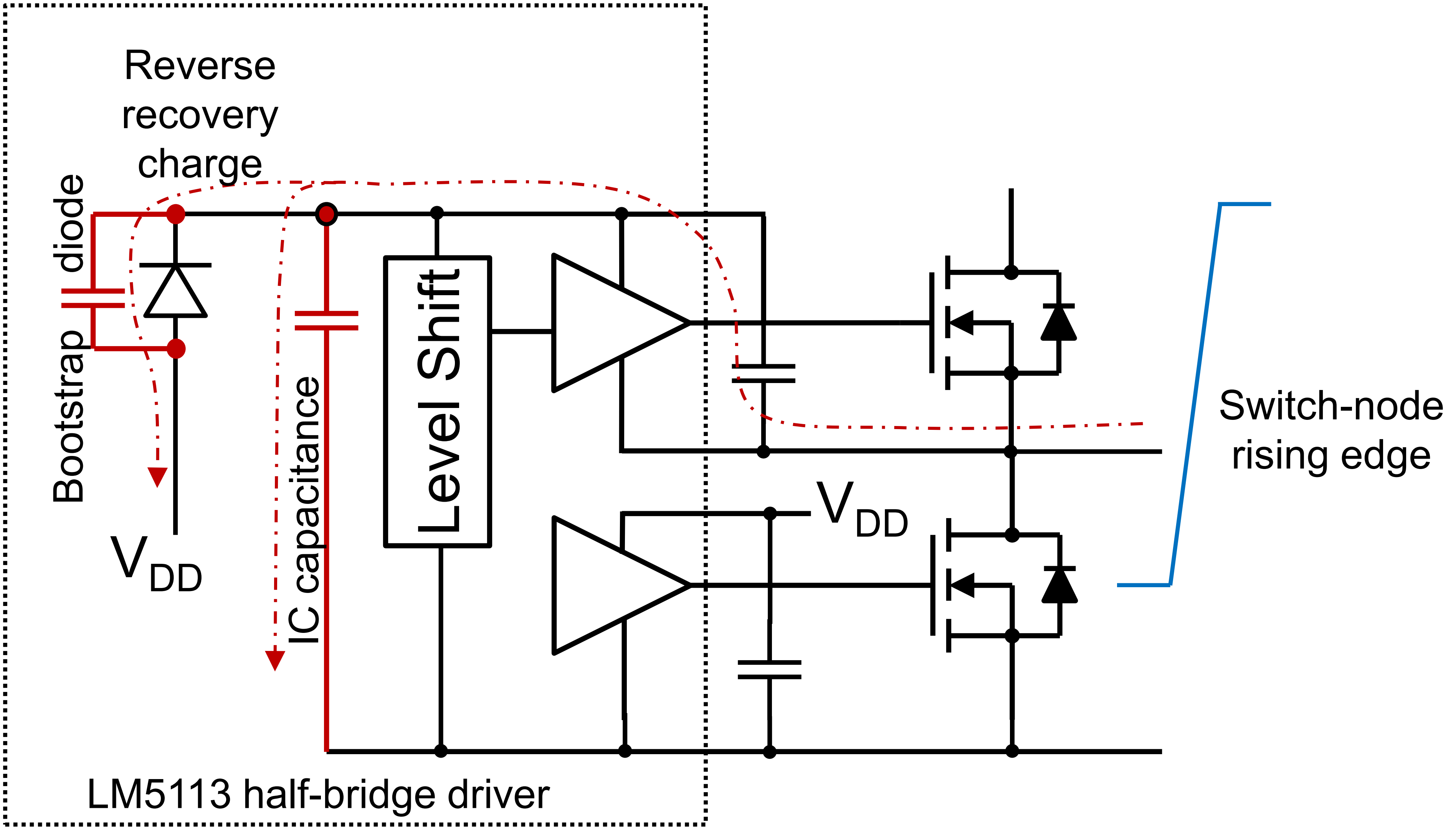
$42V_{IN}$ at $1A_{OUT}$



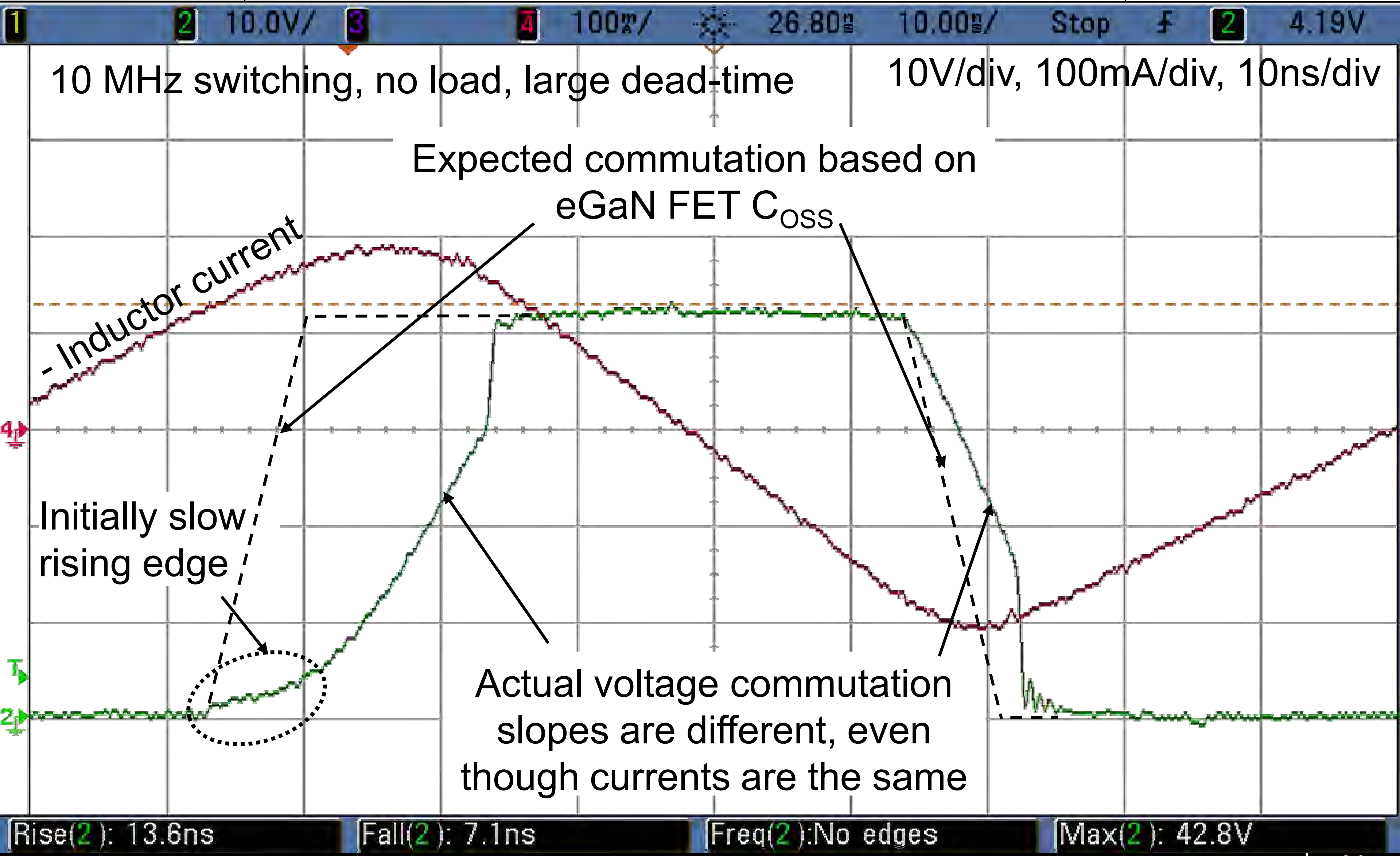
$42V_{IN}$, $20V_{OUT}$, 10MHz



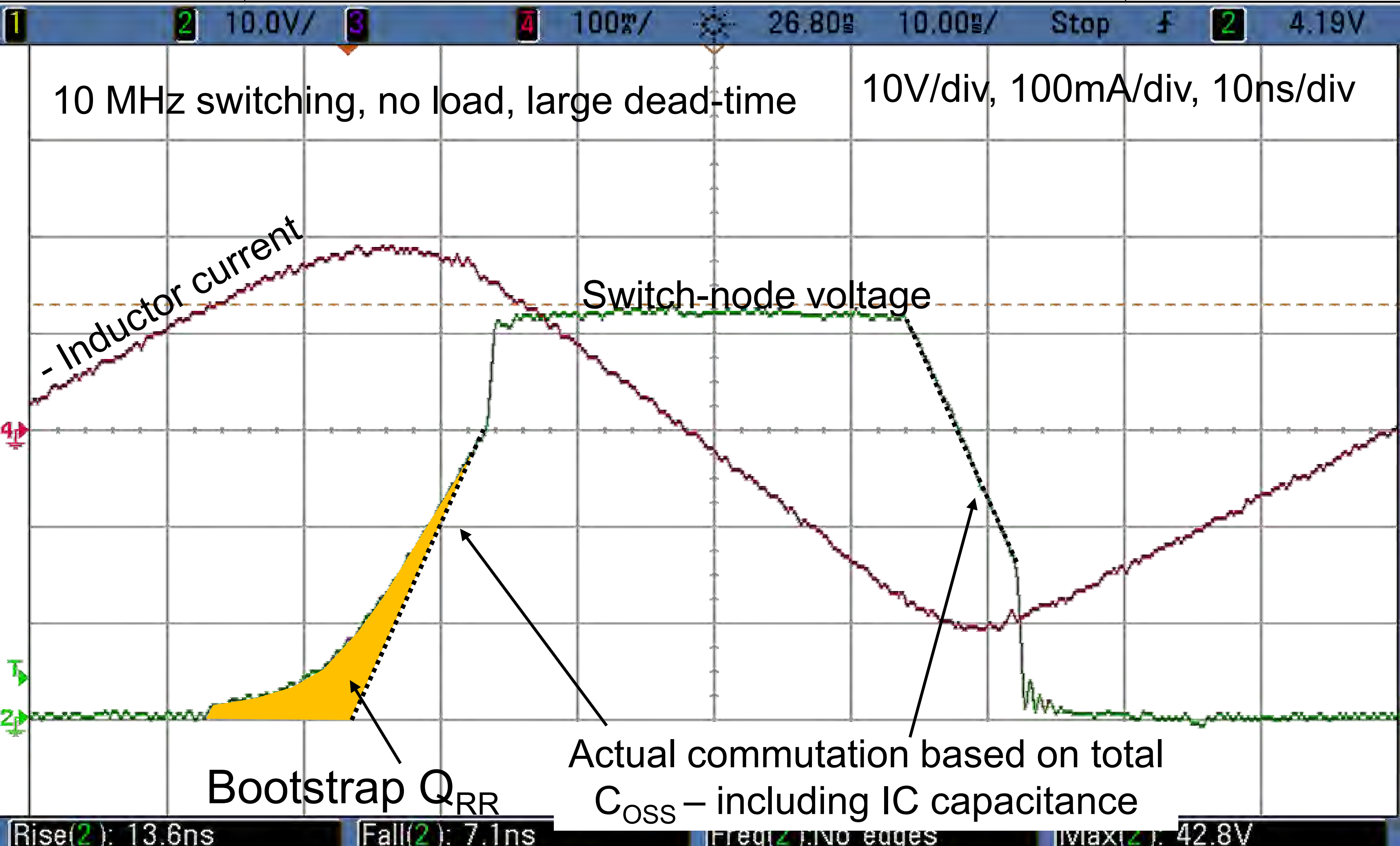
Parasitic Losses



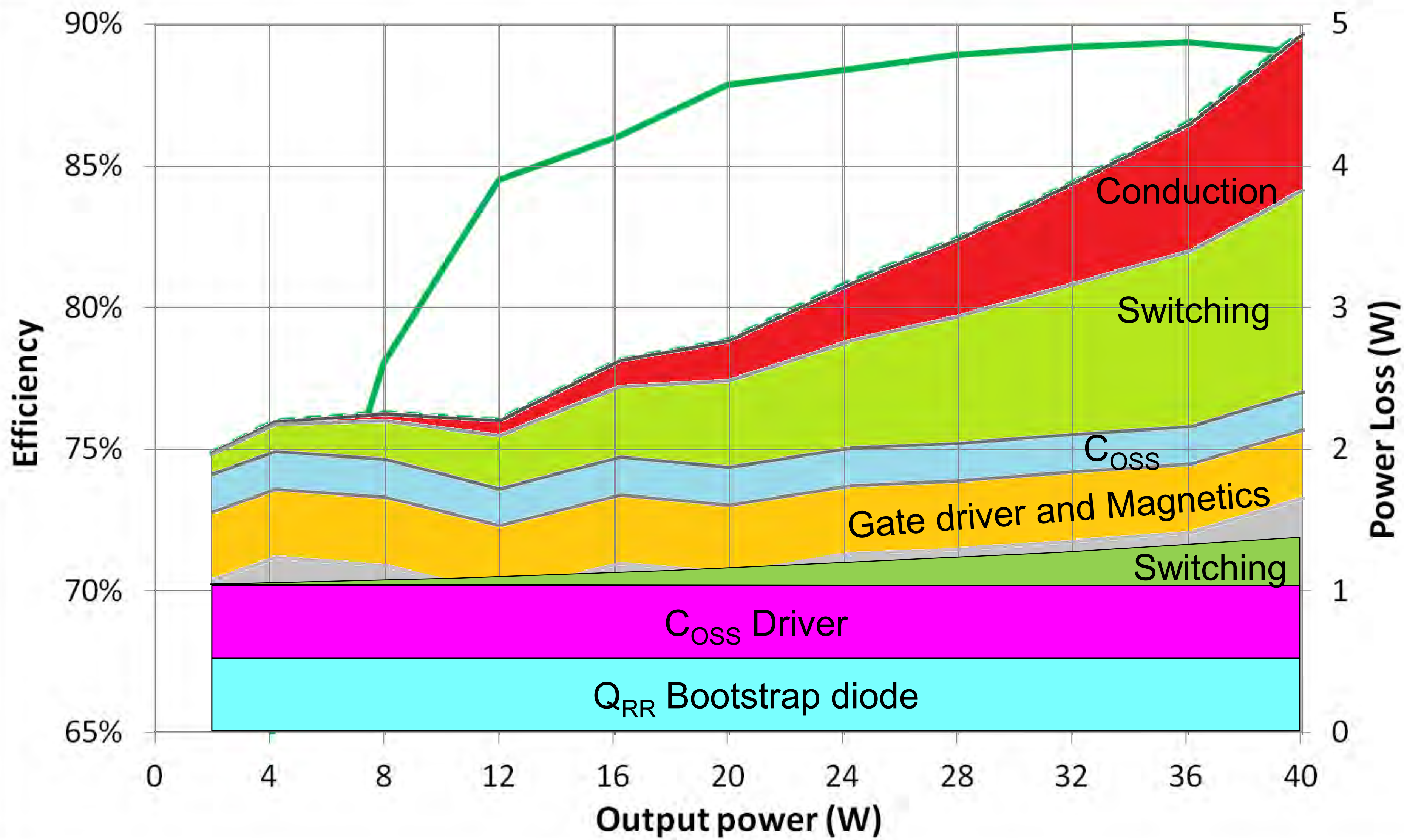
No-load Switching



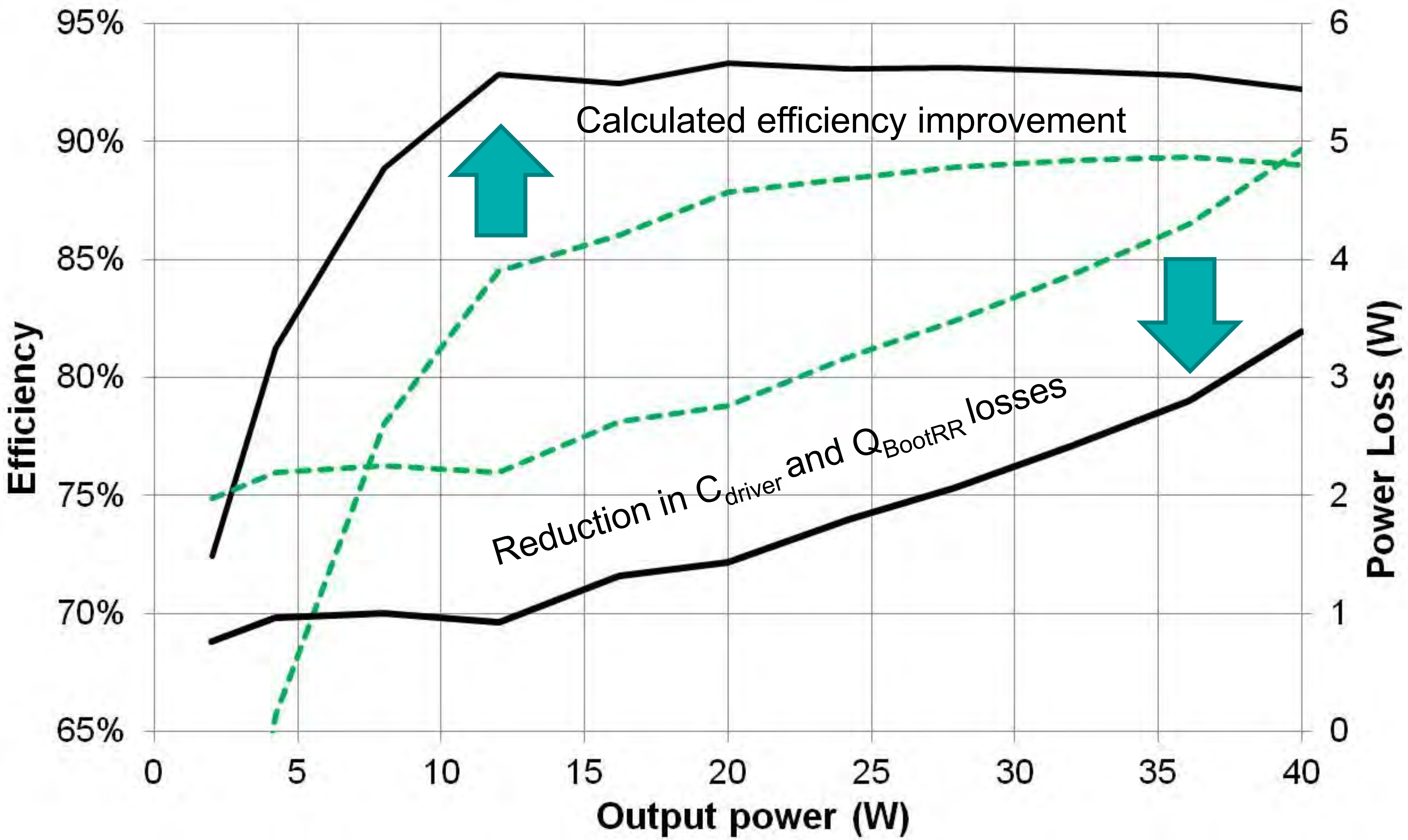
Loss Breakdown



$42V_{IN}$, $20V_{OUT}$, 10MHz



eGaN FET Limited Efficiency



Summary

- New devices enable higher switching frequencies
- Switching 42V, 40W at 10MHz at 89% possible
- Driver parasitics limit performance
  - Doubles light load losses

EPC
EFFICIENT POWER CONVERSION

The end of the road for silicon.....

is the beginning of the eGaN FET journey!